REMARKS

Claims 1-9 and 13-20 are pending. Claims 1-2 and 7-16 are allowed. Claims 3-6 and 17-20 are rejected as being anticipated by U.S. patent 5,850,537 (herein referred to as "Selvidge"). The Applicant traverses the rejection.

Fig. 3 of Selvidge shows two FPGAs 12 and 12' connected by a single physical wire 15x. Six global links 24a-f are time division multiplexed onto the single physical wire 15x by two pipeline shift loops 30a [col. 5, lines 47-52]. Thus Selvidge discloses time division multiplexed data between two ICs over a fixed serial line 15x.

Claim 3 recites an integrated circuit comprising: a set of configurable logic blocks comprising multiple signal sources and at least one destination; a time multiplexing signal generator controlling which of the multiple signal sources provides its signal to a corresponding signal destination; and a programmable interconnect coupled between an output of the time multiplexing signal generator and a destination configurable logic block. Thus claim 3 recites a time division multiplexed signal over a programmable interconnect within the single IC. As supported by the specification the programmable interconnect is hence shared between signal sources (paragraph[0012]).

As Selvidge neither discloses nor teaches intra-chip communication using a programmable interconnect versus a fixed wire, Claim 3 should be allowable.

Claims 4-6 and 17-20 being dependent upon claim 3 should be allowable for at least the same reason claim 3 is allowable.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

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If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on December 1, 2005.

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